

AMENDMENTS TO THE CLAIMS

These claims replace all prior versions and listings of claims in the above-referenced application.

1 1. (Currently Amended) A method for adapting test thresholds, comprising
2 the following steps:

3 acquiring location information for a plurality of solder joints on a printed-circuit
4 device;

5 obtaining information indicative of the variation in distance between a mounting
6 surface of the printed-circuit device and a printed-circuit board; recording a measurement
7 of a physical property of a plurality of solder joints used to couple the printed-circuit
8 device to the printed-circuit board;

9 analyzing recorded measurements of a set of neighbor solder joints to calculate a
10 range of acceptable measurements for each respective neighbor solder joint responsive to
11 variation in distance between the mounting surface of the printed-circuit device and the
12 printed-circuit board, wherein analyzing is responsive to a best fit polynomial equation
13 using the recorded measurements; and

14 setting at least one threshold responsive to the range.

1 2. (Original) The method of claim 1, wherein the step of acquiring location
2 information comprises an investigation of an array package.

1 3. (Original) The method of claim 1, wherein the step of recording
2 comprises a diameter measurement.

1 4. (Original) The method of claim 1, wherein the step of recording
2 comprises a height measurement.

1 5. (Original) The method of claim 1, wherein the step of recording
2 comprises a volume measurement.

1 6. (Currently Amended) The method of claim 1, wherein the analyzing step
2 comprises performing a statistical analysis.

1 7. (Original) The method of claim 6, wherein the statistical analysis
2 comprises calculating the median of the recorded measurements of the identified set of
3 neighbor solder joints.

1 8. (Canceled)

1 9. (Currently Amended) The method of claim 1, wherein the estimating step
2 comprises applying the recorded measurements of a plurality of solder joints in a Fourier
3 analysis.

1 10. (Original) The method of claim 9, wherein the Fourier analysis comprises
2 the application of a high-frequency filter on the recorded measurements of an identified
3 set of solder joints distributed across the surface of the device.

1 11. (Currently Amended) The method of claim 1, wherein the step of setting
2 further comprises:
3 comparing the expected value with the recorded measurement to generate an error
4 value for the plurality of solder joints on the printed-circuit device; and
5 performing an outlier analysis on the plurality of error values to establish at least
6 one threshold value.

1 12. (Currently Amended) The method of claim 11, wherein the step of
2 comparing the expected value with the recorded measurement comprises a mathematical
3 combination of the expected value with the recorded measurement.

1 13. (Original) The method of claim 12, wherein the mathematical
2 combination comprises a difference.

1 14. (Currently Amended) A method for identifying solder joint defects,
2 comprising the steps of:
3 recording a measurement associated with a plurality of solder joints on a printed-
4 circuit device;

5 analyzing the measurement associated with each of a set of neighboring solder
6 joints to calculate an expected value for the measurement associated with each of the
7 solder joints that accounts for acceptable variance in the distance between the mounting
8 surfaces of a printed-circuit device and a printed-circuit board coupled by the solder
9 joints, wherein analyzing is responsive to a best fit polynomial equation using the
10 recorded measurements;

11 comparing the recorded measurement with the expected value for the plurality of
12 solder joints to generate a respective error value; and

13 identifying defective solder joints by applying an error value outlier analysis to
14 the plurality of error values.

1 15. (Currently Amended) The method of claim 14, wherein the step of
2 recording comprises an investigation of an array package.

1 16. (Currently Amended) The method of claim 14, wherein the step of
2 recording comprises a diameter measurement.

1 17. (Currently Amended) The method of claim 14, wherein the step of
2 analyzing an expected value for the plurality of solder joints comprises performing a
3 statistical analysis.

1 18. (Currently Amended) The method of claim 14, wherein the step of
2 estimating an expected value for the plurality of solder joints comprises performing a
3 statistical analysis on the recorded measurements of a set of solder joints equidistant
4 from the centroid of the printed-circuit device.

1 19. (Original) The method of claim 17, wherein the statistical analysis
2 comprises calculating the median of the recorded measurements of the identified set of
3 neighboring solder joints.

1 20. (Cancelled)

1 21. (Currently Amended) The method of claim 14, wherein ~~the step of~~
2 estimating an expected value for the plurality of solder joints comprises applying the
3 recorded measurements of a plurality of solder joints in a Fourier analysis.

1 22. (Original) The method of claim 21, wherein the Fourier analysis
2 comprises the application of a high-frequency filter on the recorded measurements of a
3 plurality of solder joints.

1 23. (Currently Amended) The method of claim 14, wherein ~~the step of~~
2 comparing the expected value with the recorded measurement comprises a mathematical
3 combination of the expected value with the respective recorded measurement.

1 24. (Original) The method of claim 23, wherein the mathematical
2 combination comprises the difference of the expected value with the respective recorded
3 measurement.

1 25. (Currently Amended) The method of claim 23, wherein ~~the step of~~
2 identifying defective solder joints comprises a box plot analysis responsive to the
3 plurality of error values.

1 26. (Currently Amended) An improved solder-joint inspection system,
2 comprising:
3 means for measuring at least one characteristic of a plurality of solder joints
4 located within a select area of a printed-circuit device;
5 means for computing an expected value for the measured characteristic for each
6 of the plurality of solder joints that varies as a function of distance between the mounting
7 surface of the printed-circuit device and a printed-circuit board over the select area of the
8 printed circuit device, wherein computing an expected value is responsive to a best fit
9 polynomial equation using the measurements; and
10 means for formulating an error value as a function of the measured characteristic
11 and the expected value for the plurality of solder joints.

1 27. (Original) The system of claim 26, further comprising:
2 means for analyzing the plurality of error values to identify solder joint defects.

1 28. (Original) The system of claim 27, wherein the means for analyzing
2 comprises a box plot.

1 29. (Original) The system of claim 26, wherein the means for measuring
2 comprises an automated X-ray inspection system.

1 30. (Original) The system of claim 26, wherein the means for measuring
2 comprises an optical inspection system.

1 31. (Currently Amended) A solder-joint defect analysis detection program
2 stored on a computer-readable medium, comprising:
3 logic configured to record at least one characteristic of a plurality of solder joints
4 located within a select area of a printed-circuit device;
5 logic configured to determine an expected value for the at least one characteristic
6 for the plurality of solder joints responsive to low frequency change in a solder joint
7 characteristics across the device;
8 logic configured to generate an error value from a mathematical combination of
9 the expected value and the recorded characteristic for the plurality of solder joints on the
10 printed-circuit device; and
11 logic configured to identify error value outliers using a box plot analysis.

1 32. (Original) The program of claim 31, wherein the logic configured to
2 record records at least one characteristic of a solder joint associated with an array
3 package.

1 33. (Original) The program of claim 31, wherein the logic configured to
2 determine an expected value reflects a statistical analysis of the recorded characteristic.

1 34. (Original) The program of claim 31, wherein the statistical analysis
2 comprises calculating a median.

1 35. (Original) The program of claim 31, wherein the logic configured to
2 generate an error value calculates the difference of the recorded characteristic and the
3 expected value.

1 36. (Canceled)

1 37. (Currently Amended) The program of claim 36 31, wherein the box plot
2 analysis identifies error values that exceed a constant multiple of the interquartile range
3 for the error values above a constant percentage of the error value data range.

1 38. (Original) The method of claim 1, wherein the step of obtaining
2 comprises measuring the distance between a mounting surface of the printed-circuit
3 device and a printed-circuit at a plurality of locations.

1 39. (Original) The method of claim 1, wherein the step of acquiring location
2 information comprises an investigation of a quad flat pack package.

1 40. (Original) The method of claim 1, wherein the step of recording
2 comprises a two-dimensional measurement.

1 41. (Original) The method of claim 1, wherein the step of recording
2 comprises a three-dimensional measurement.

1 42. (Original) The method of claim 14, wherein the step of recording
2 comprises an investigation of a quad flat pack package.

1 43. (Original) The method of claim 14, wherein the step of recording
2 comprises a one-dimensional measurement.

1 44. (Original) The method of claim 14, wherein the step of recording
2 comprises a two-dimensional measurement.

1 45. (Original) The method of claim 14, wherein the step of recording
2 comprises a three-dimensional measurement.

1 45. (Previously Presented) The method of claim 6, wherein the statistical
2 analysis is performed on a set of solder joints equidistant from the centroid of the
3 printed-circuit device.

1 47. (Previously Presented) The program of claim 32, wherein the logic
2 configured to determine an expected value is responsive to the distance between the
3 mounting surface of a printed-circuit device and a printed circuit board.